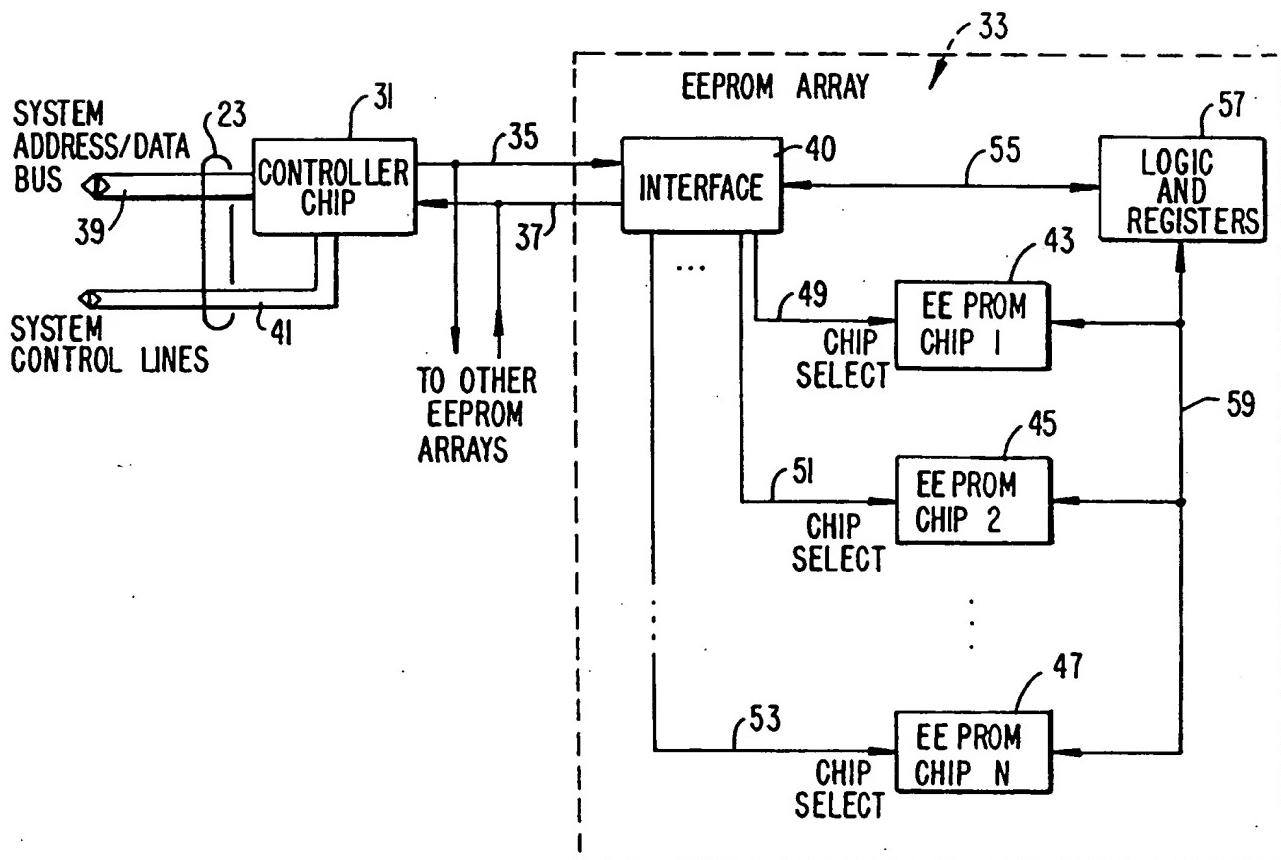
**FIG._1A**

OSCAR'S DESIGN

**FIG._1B**

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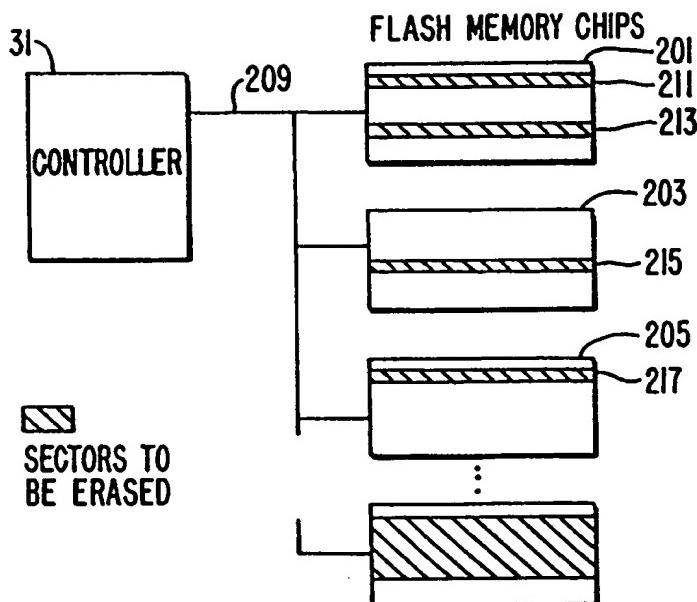


FIG._2

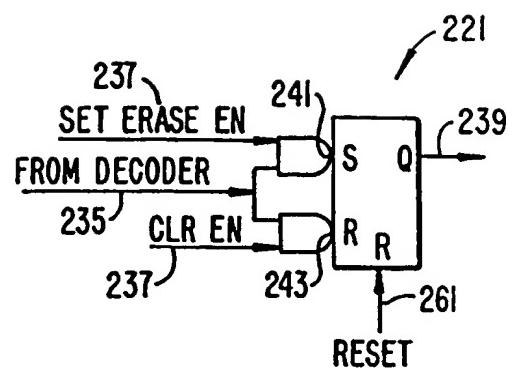


FIG._3B

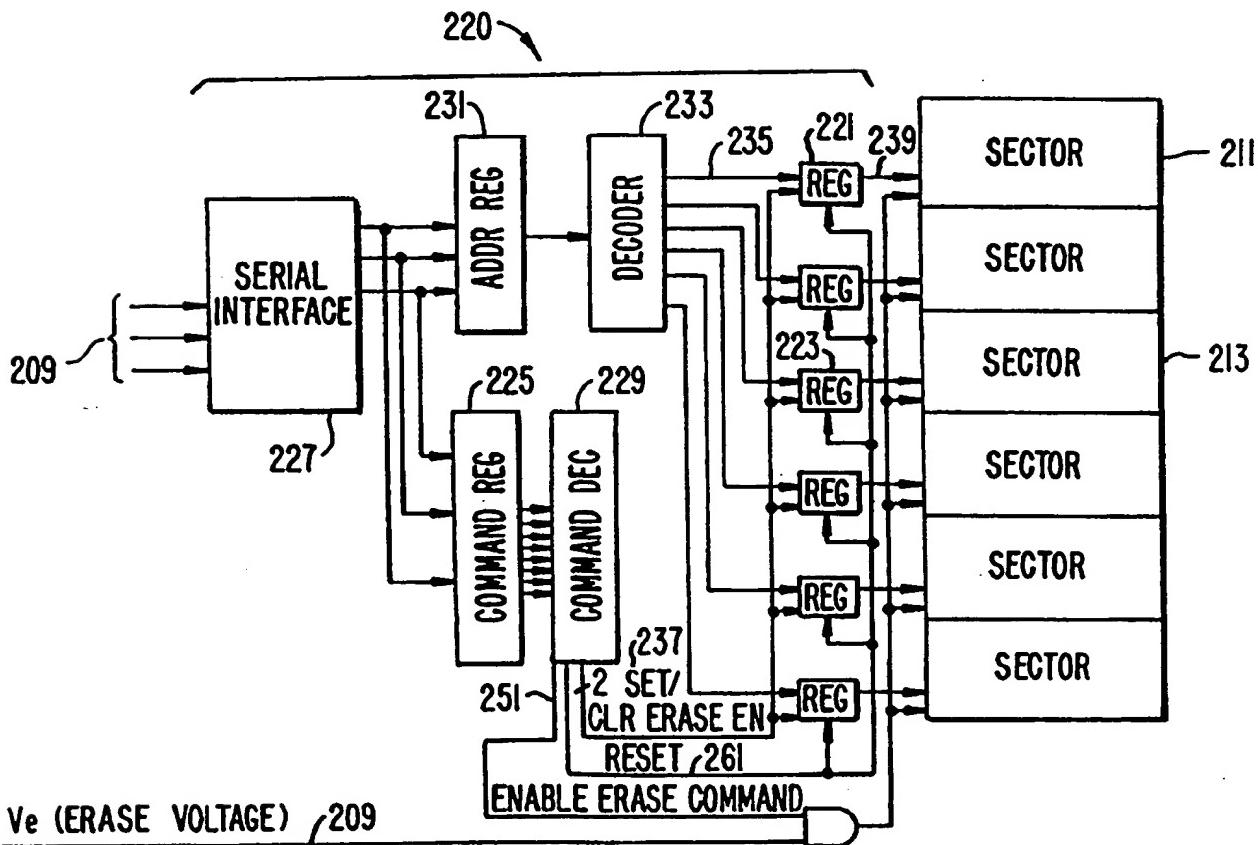


FIG._3A

TOP SECRET//COMINT

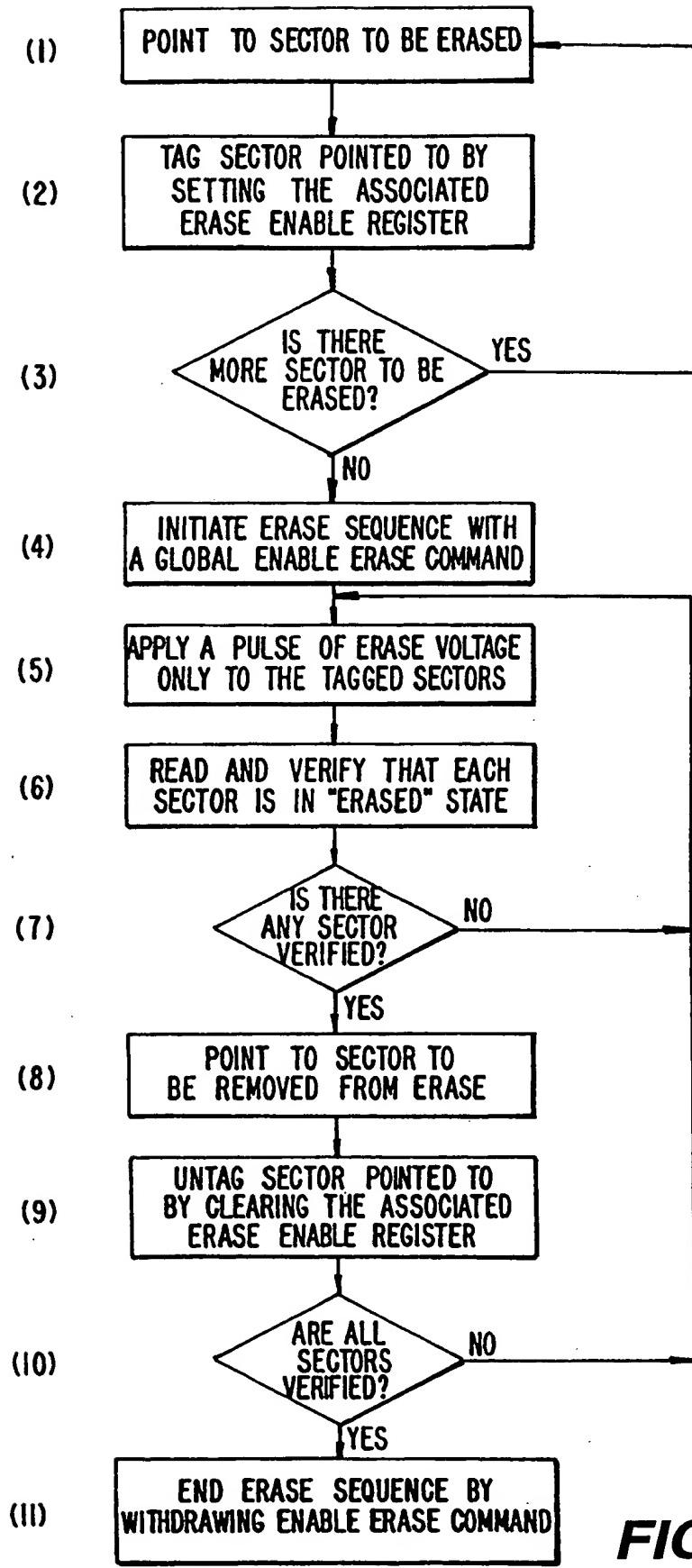
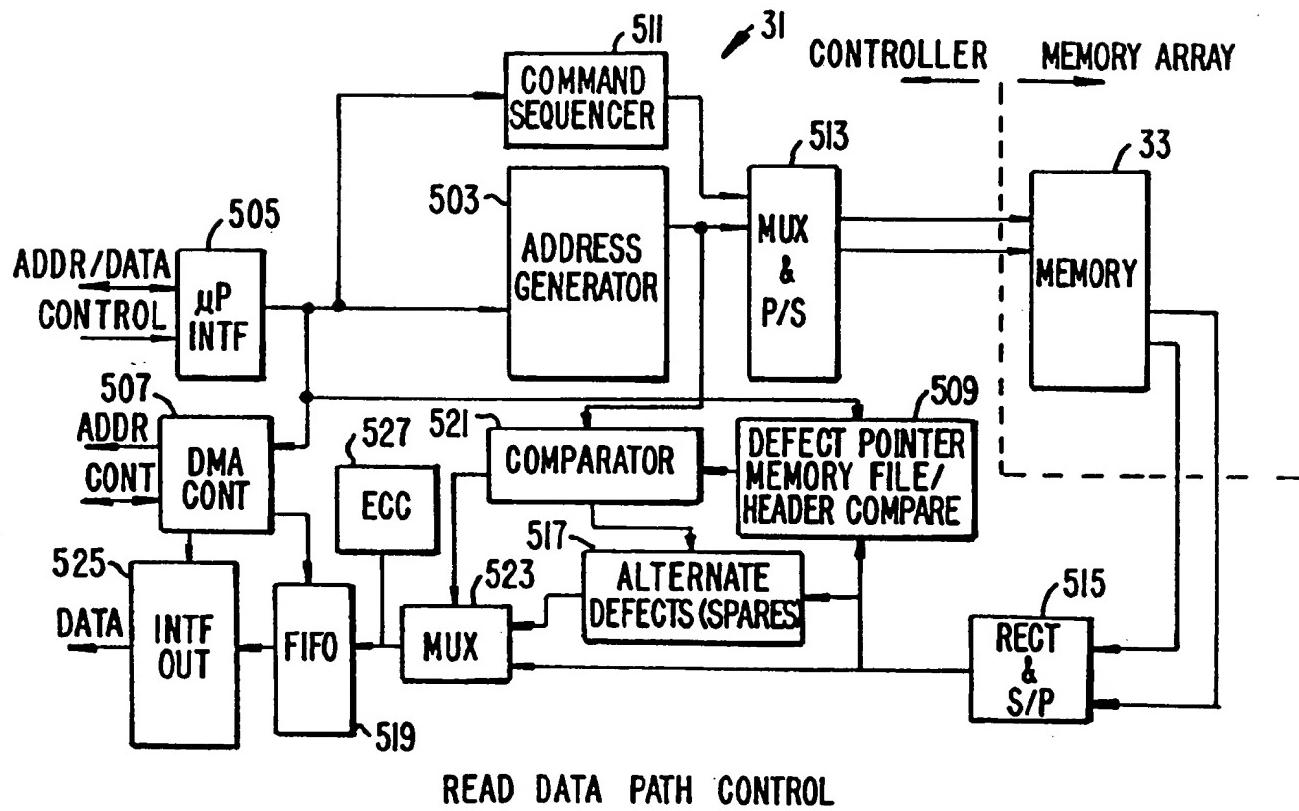
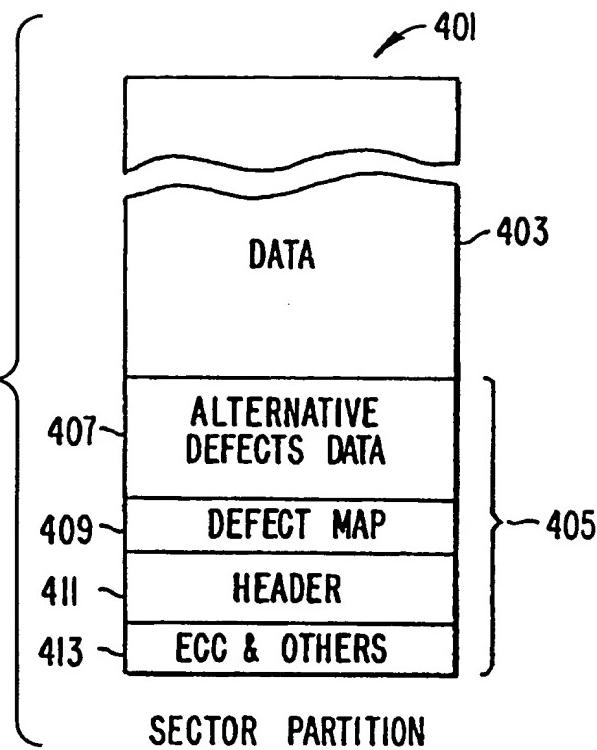


FIG._4

FIG._5**FIG._6**

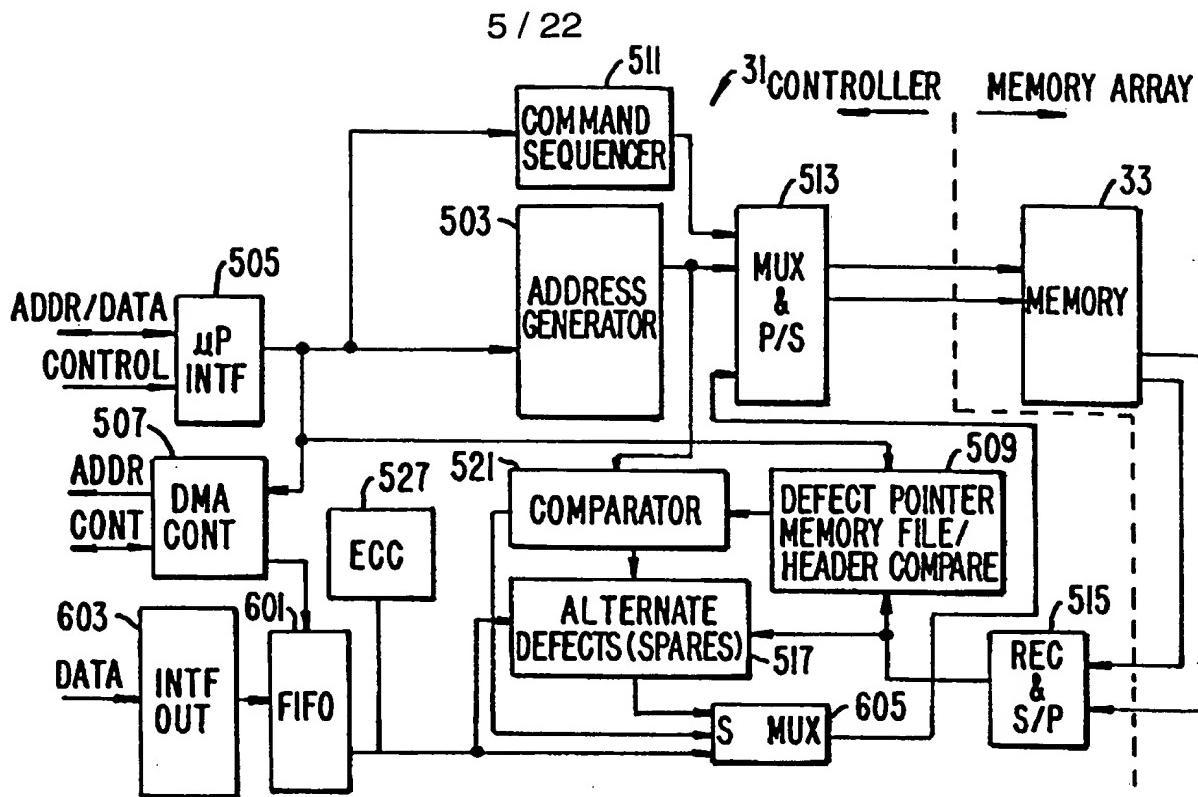
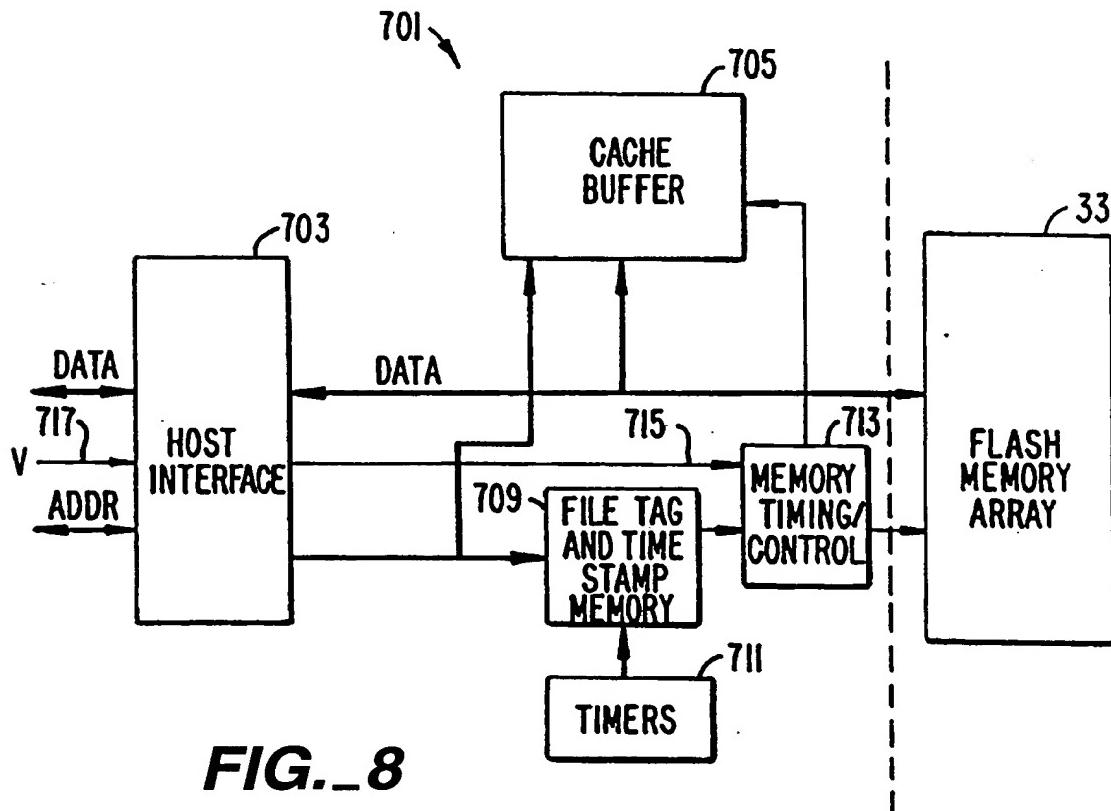
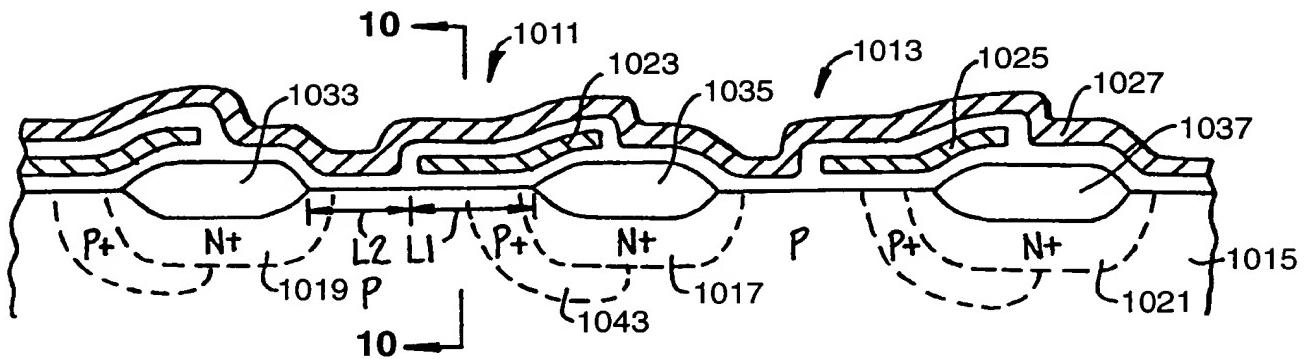
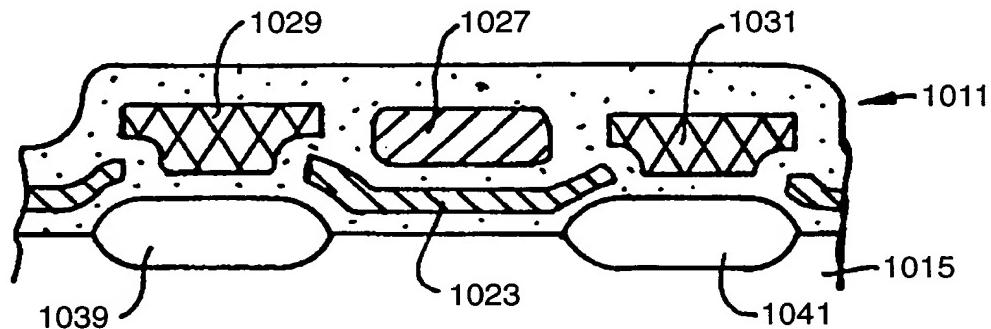
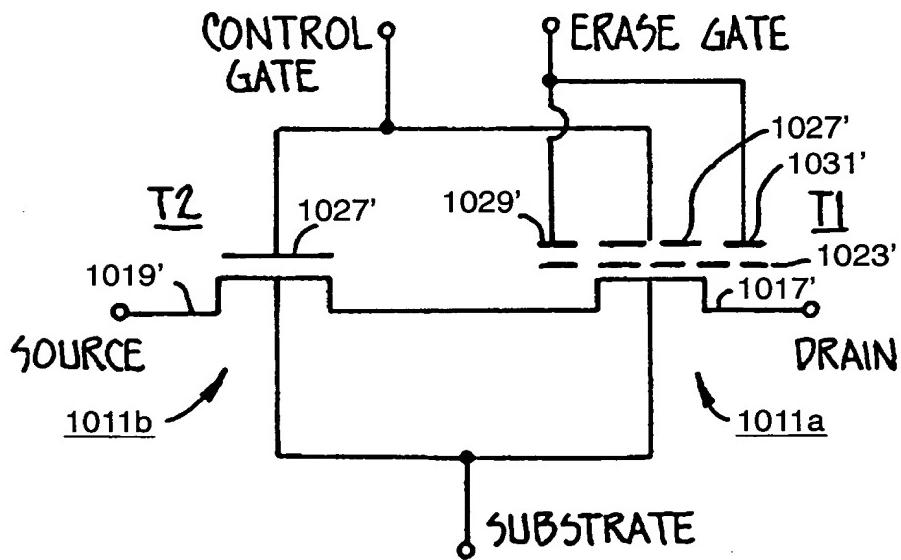


FIG._7



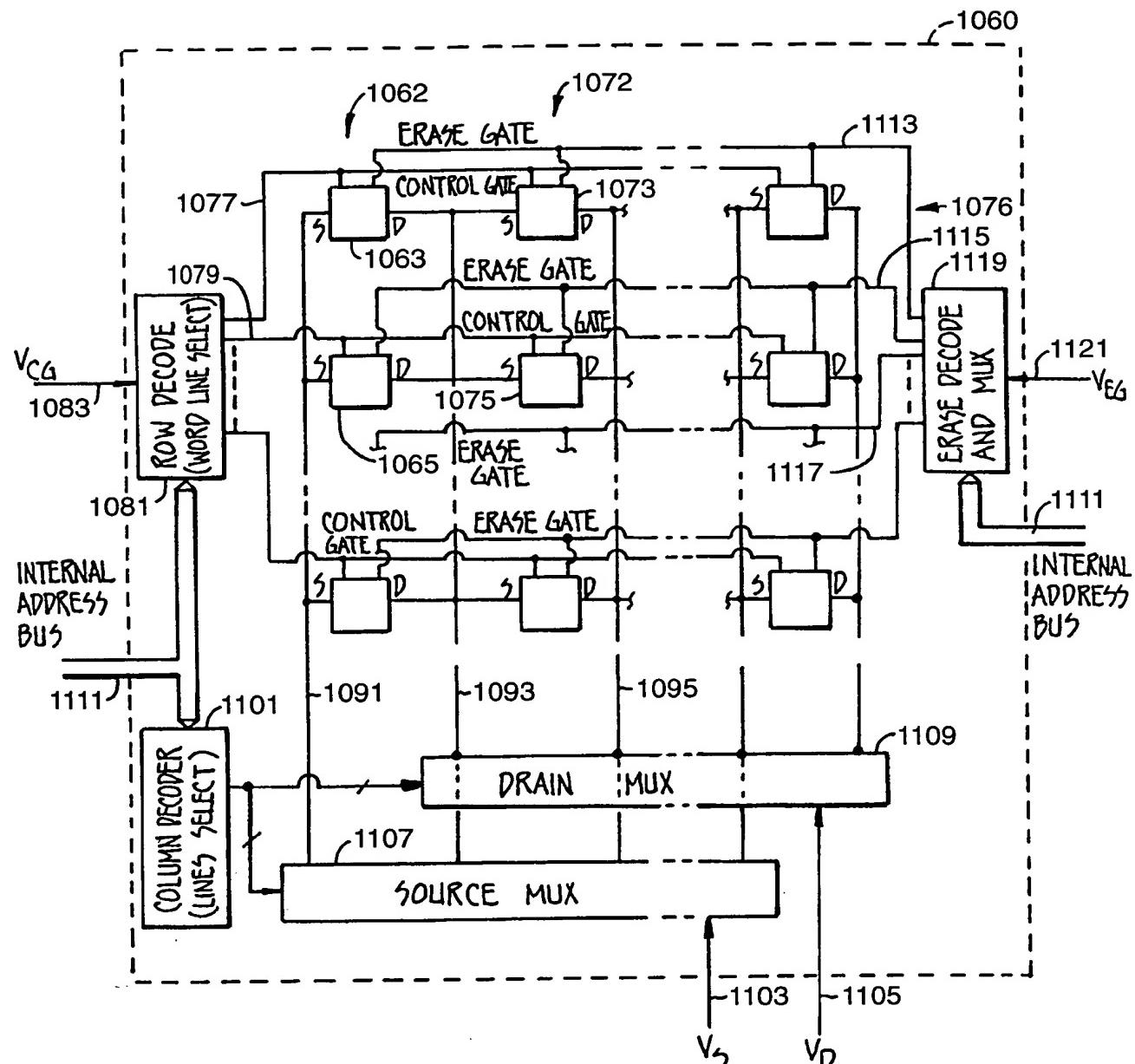
**FIG. 9**

00000000000000000000000000000000

**FIG. 10****FIG. 11**

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**FIG._ 12**

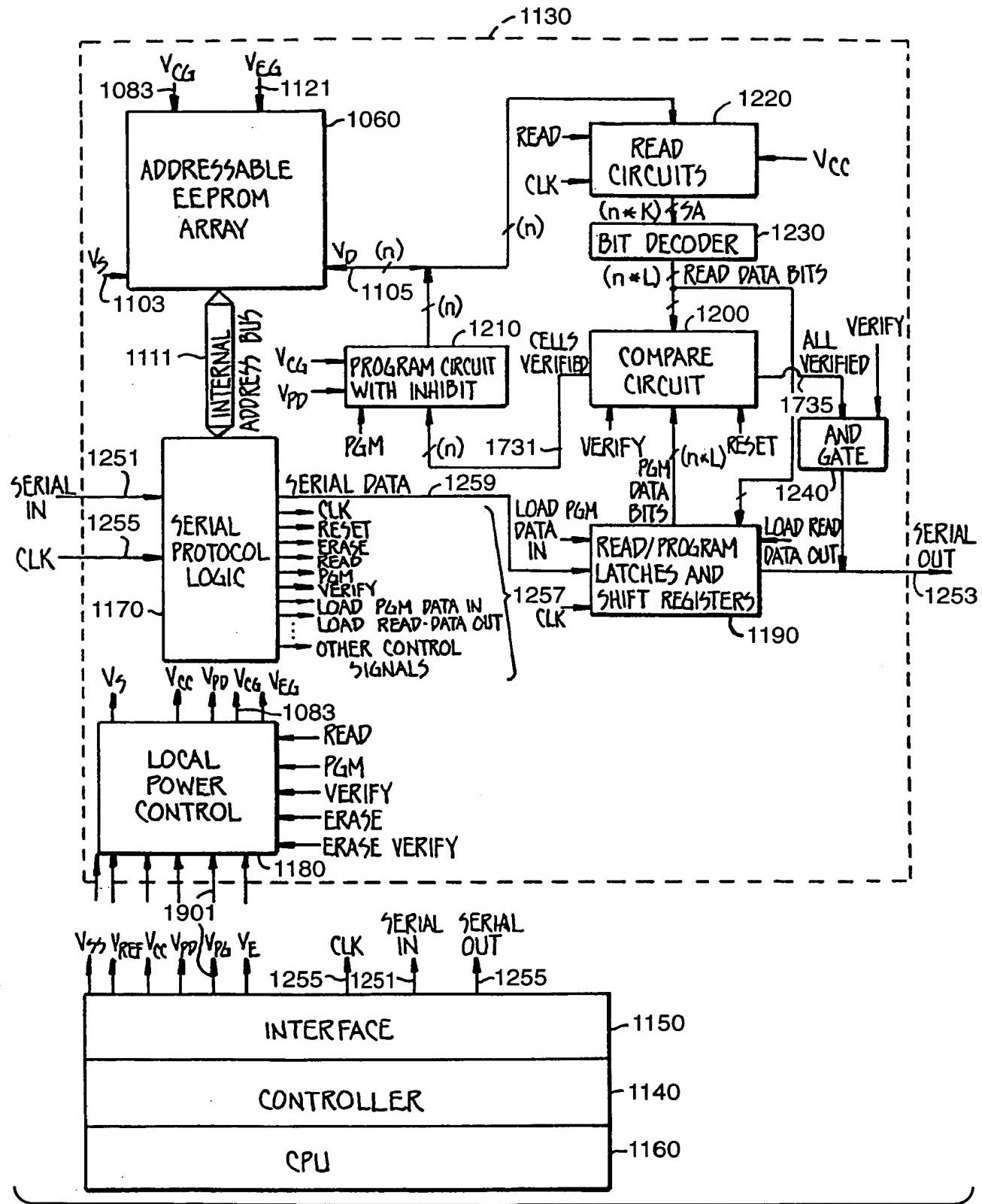
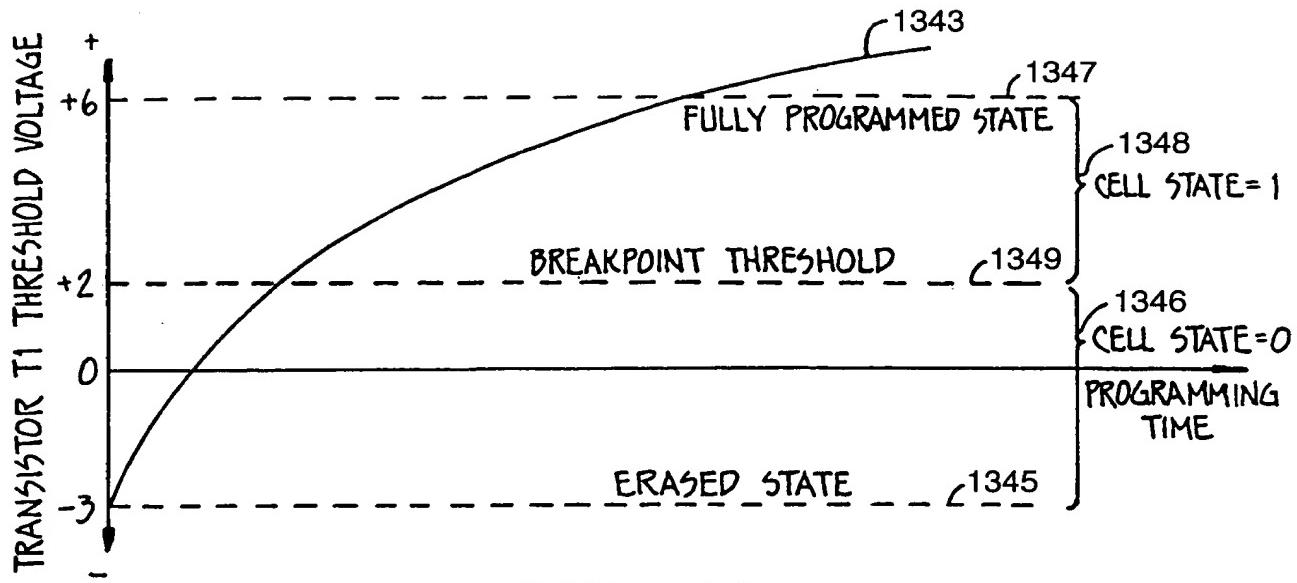
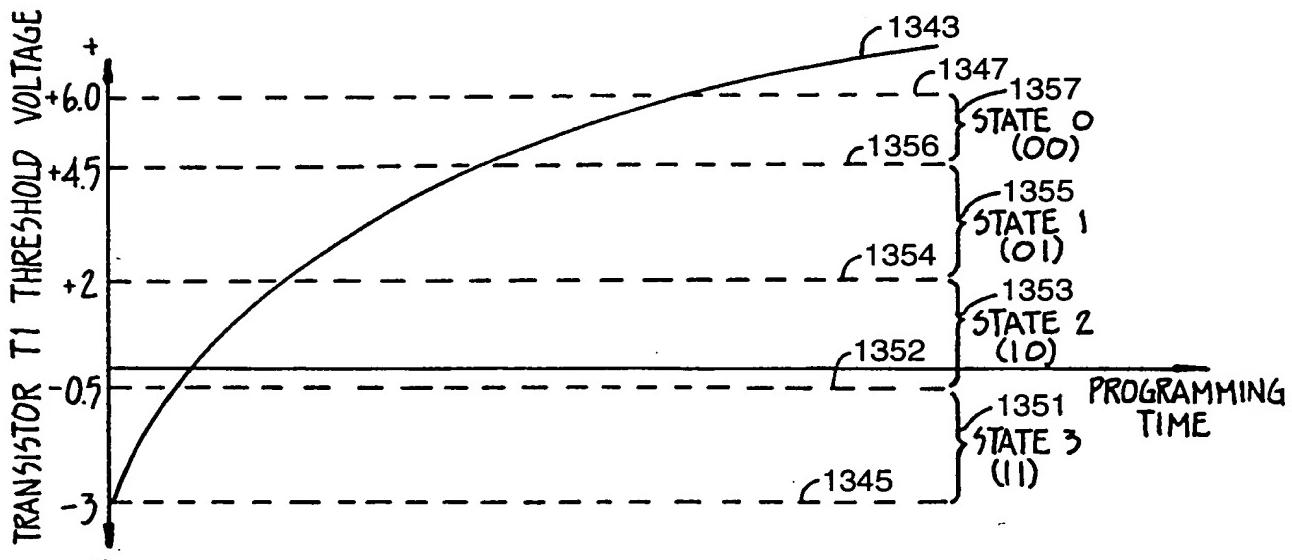


FIG.-13

**FIG._ 14****FIG._ 15A**

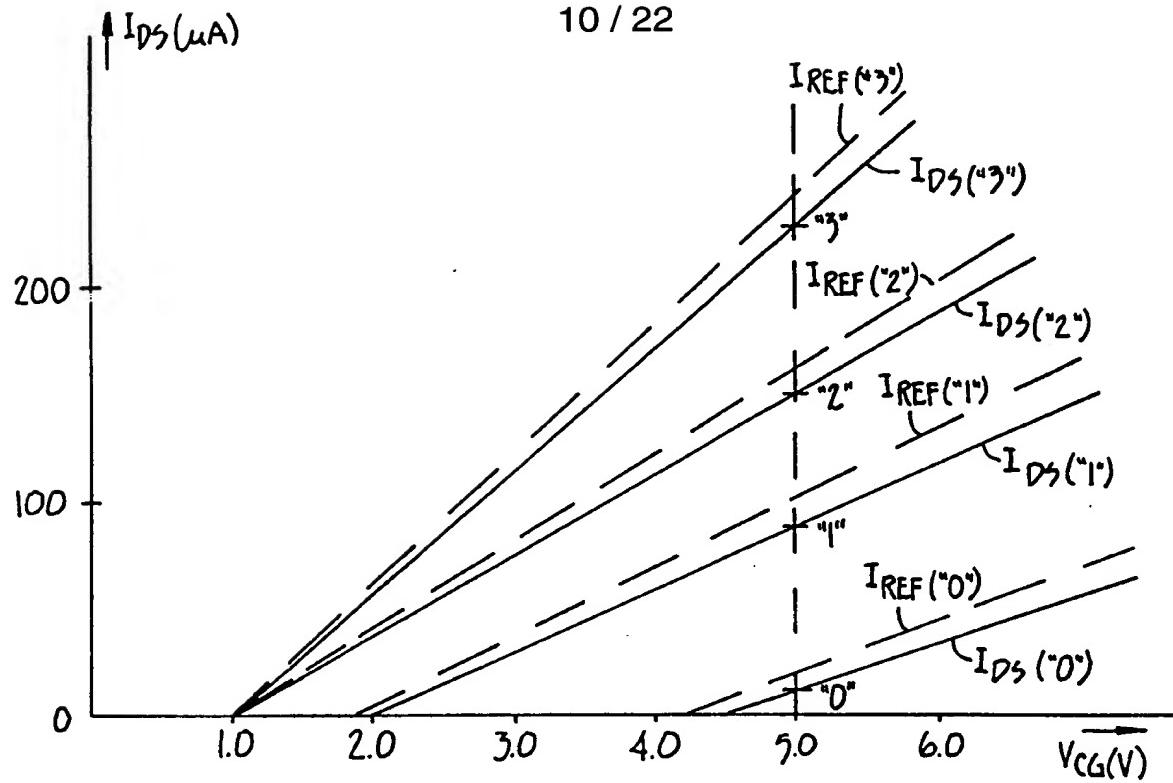


FIG._ 15B

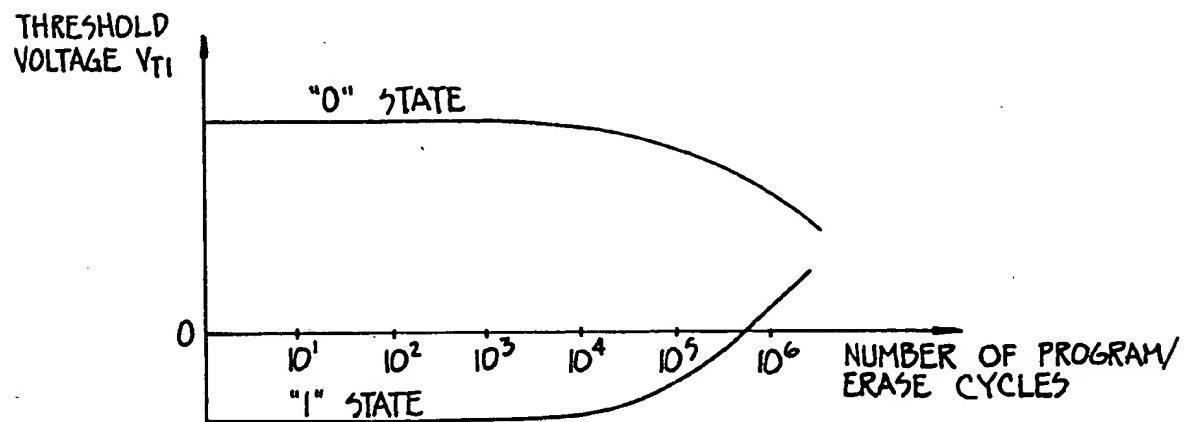


FIG._ 16A

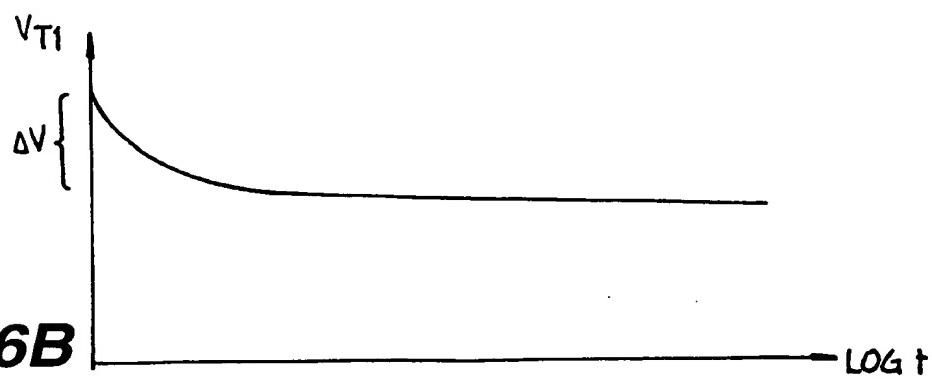
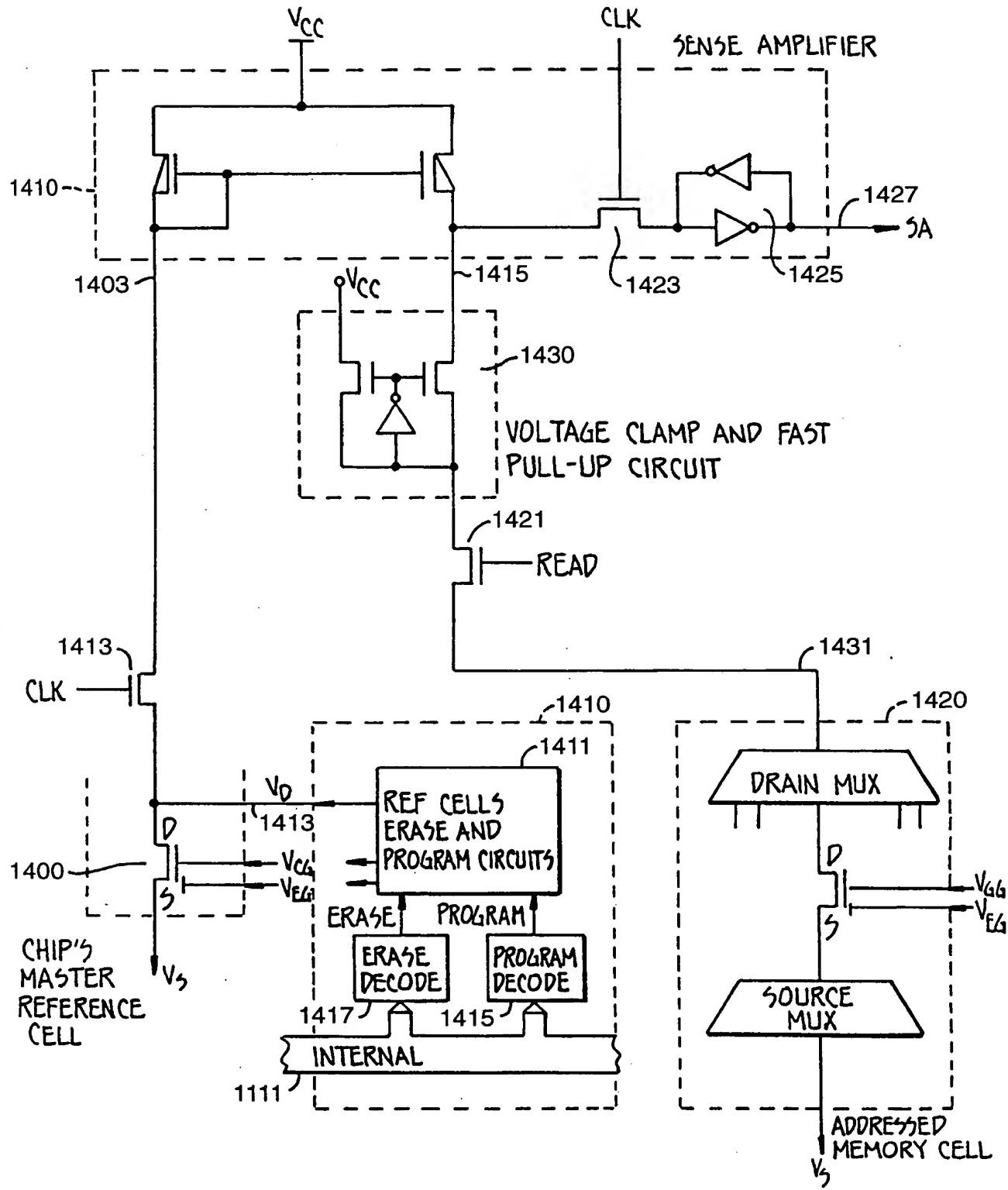
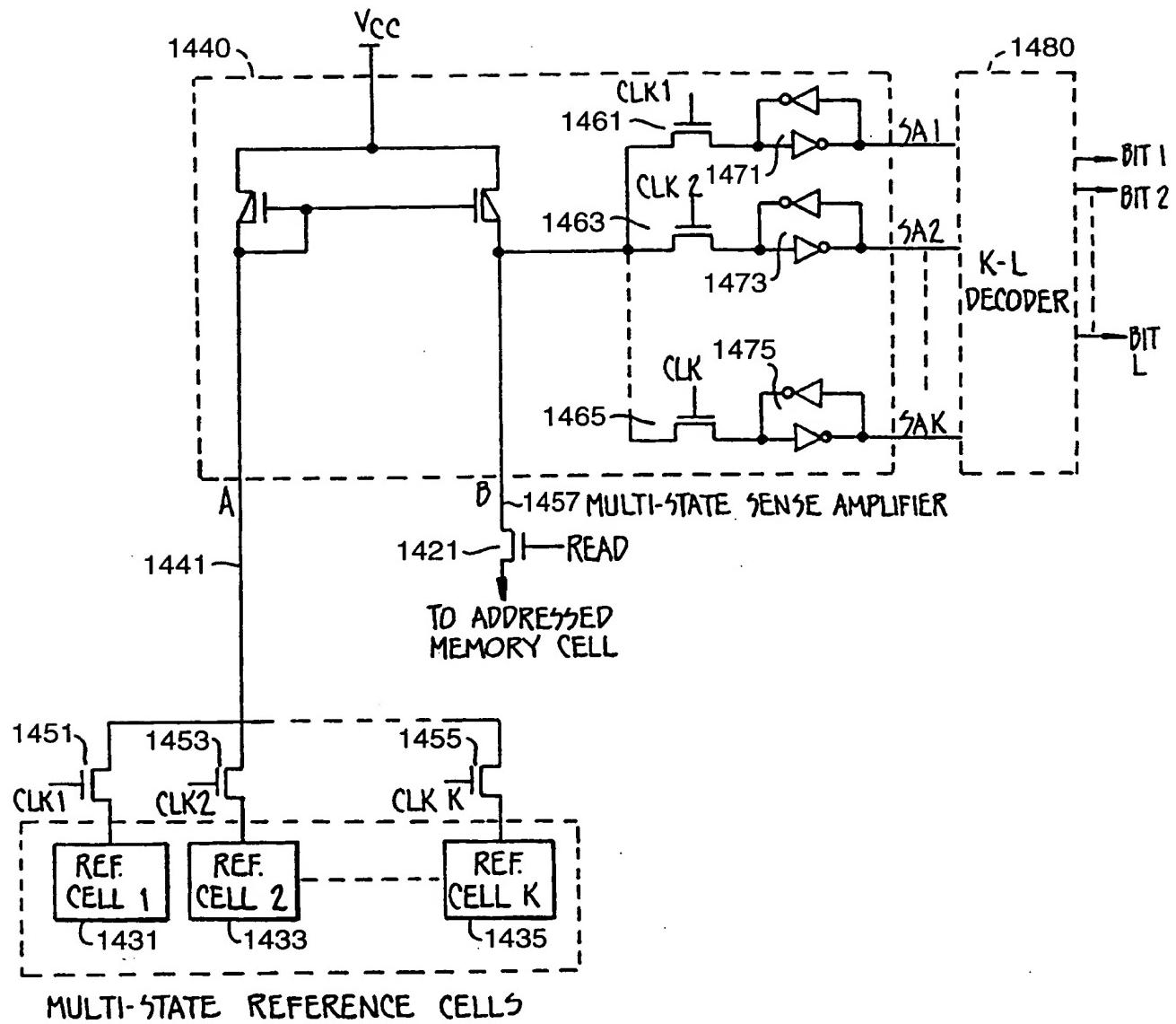
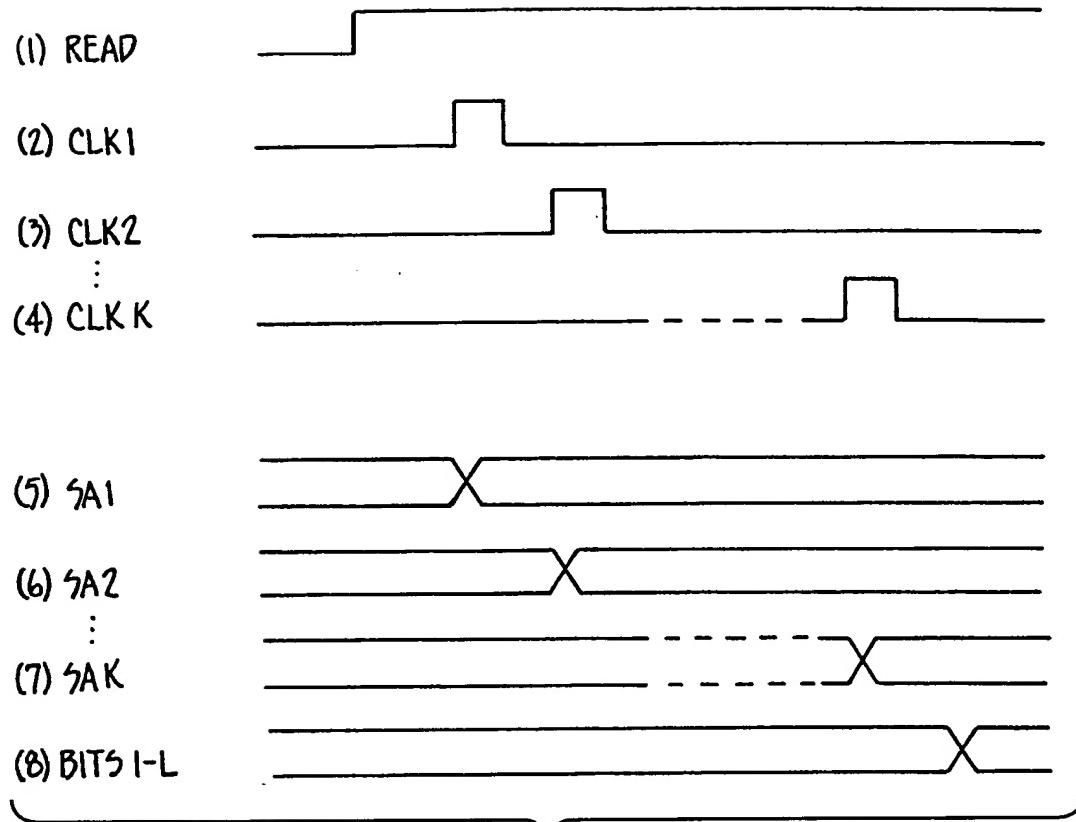
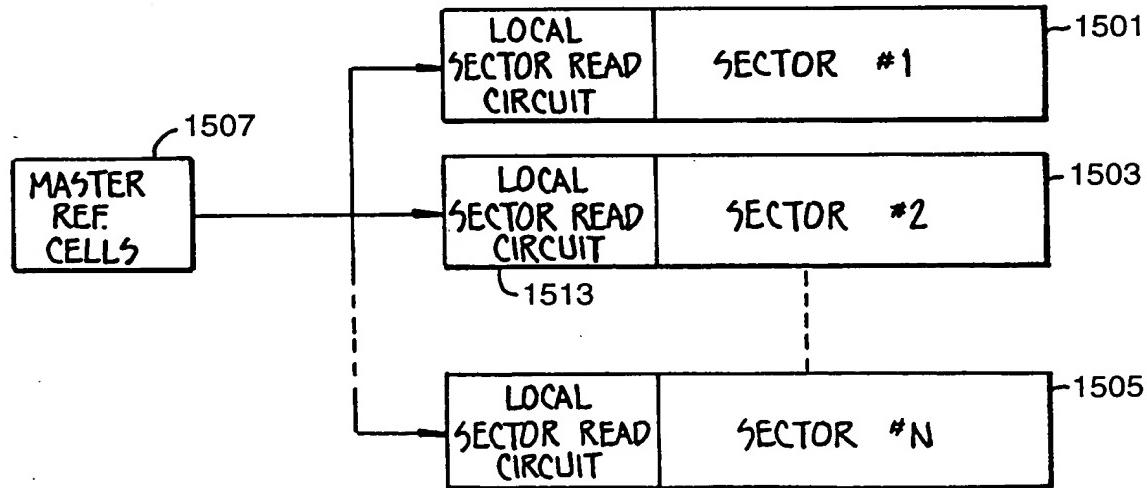


FIG._ 16B

**FIG._ 17A**

DRAFT - DO NOT CITE

**FIG._ 17B**

**FIG._ 17C****FIG._ 18**

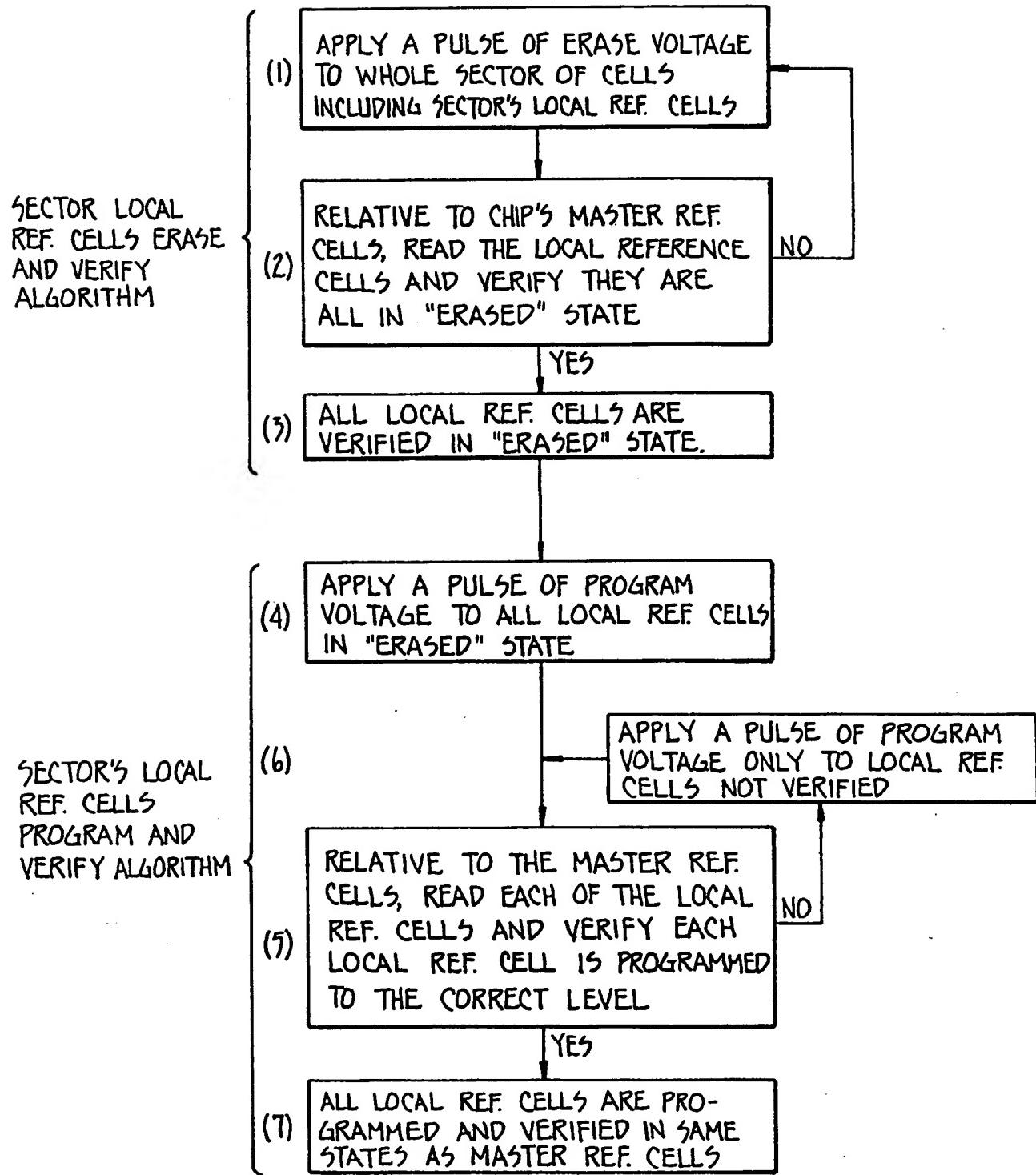
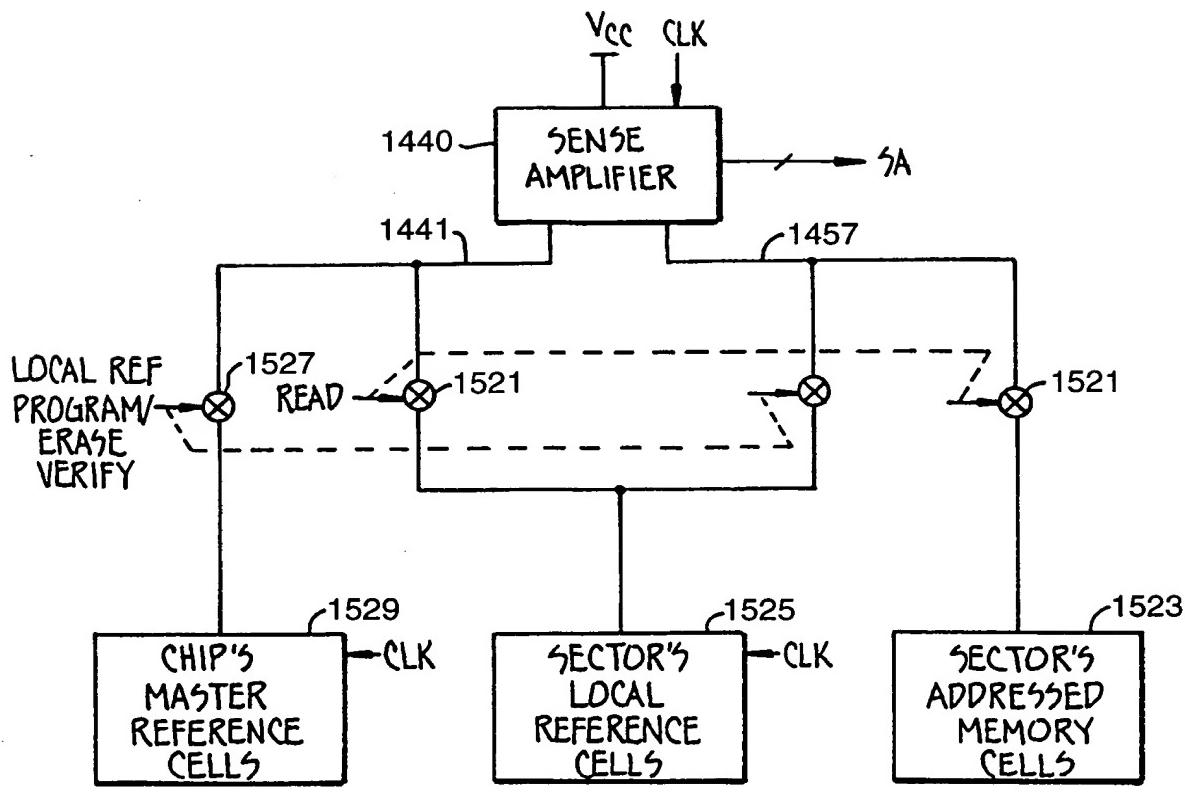


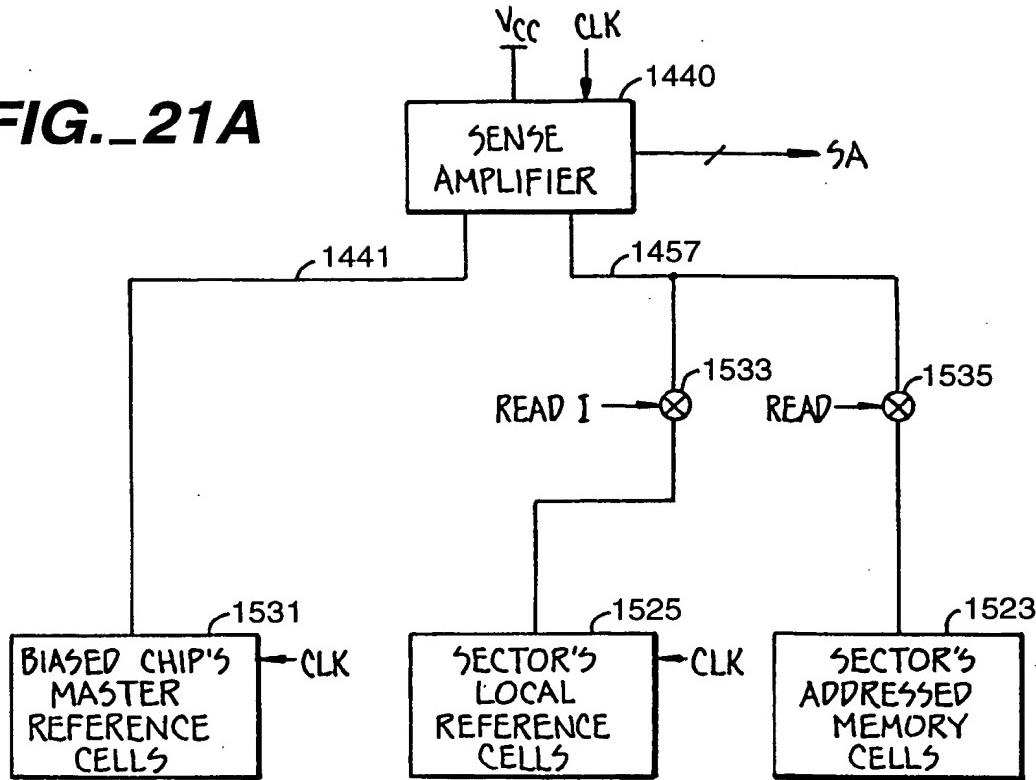
FIG._19

**FIG._20A**

LOCAL REF. CELLS ARE PREVIOUSLY PROGRAMMED
AND VERIFIED IN SAME STATES AS MASTER REF. CELLS

RELATIVE TO THE LOCAL REF. CELLS,
READ THE ADDRESSED CELLS

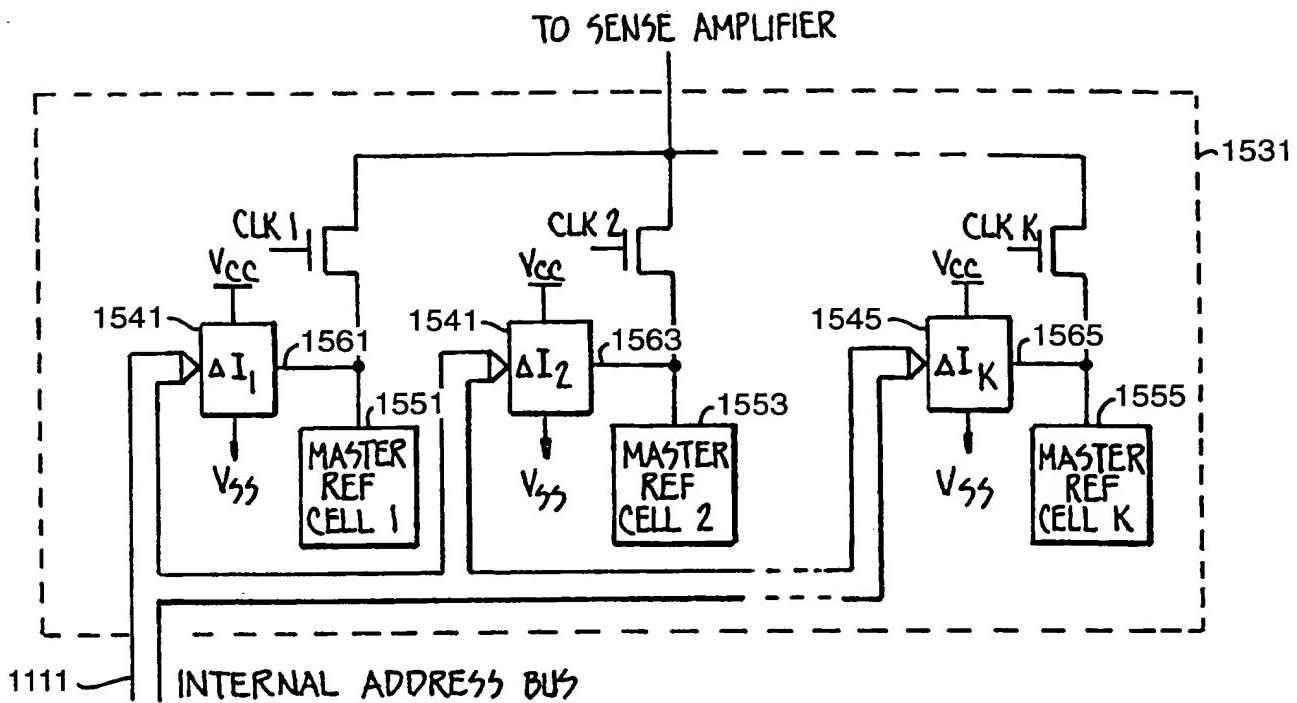
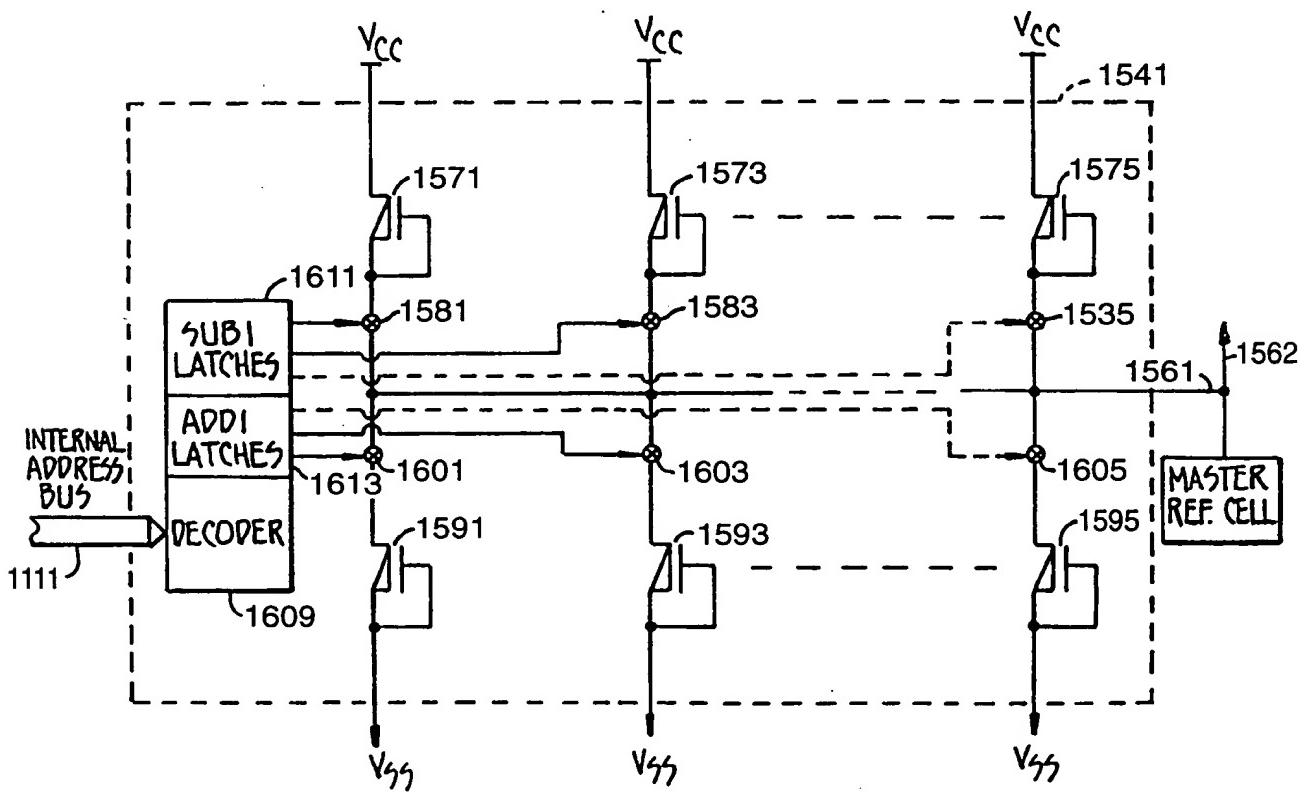
FIG._20B

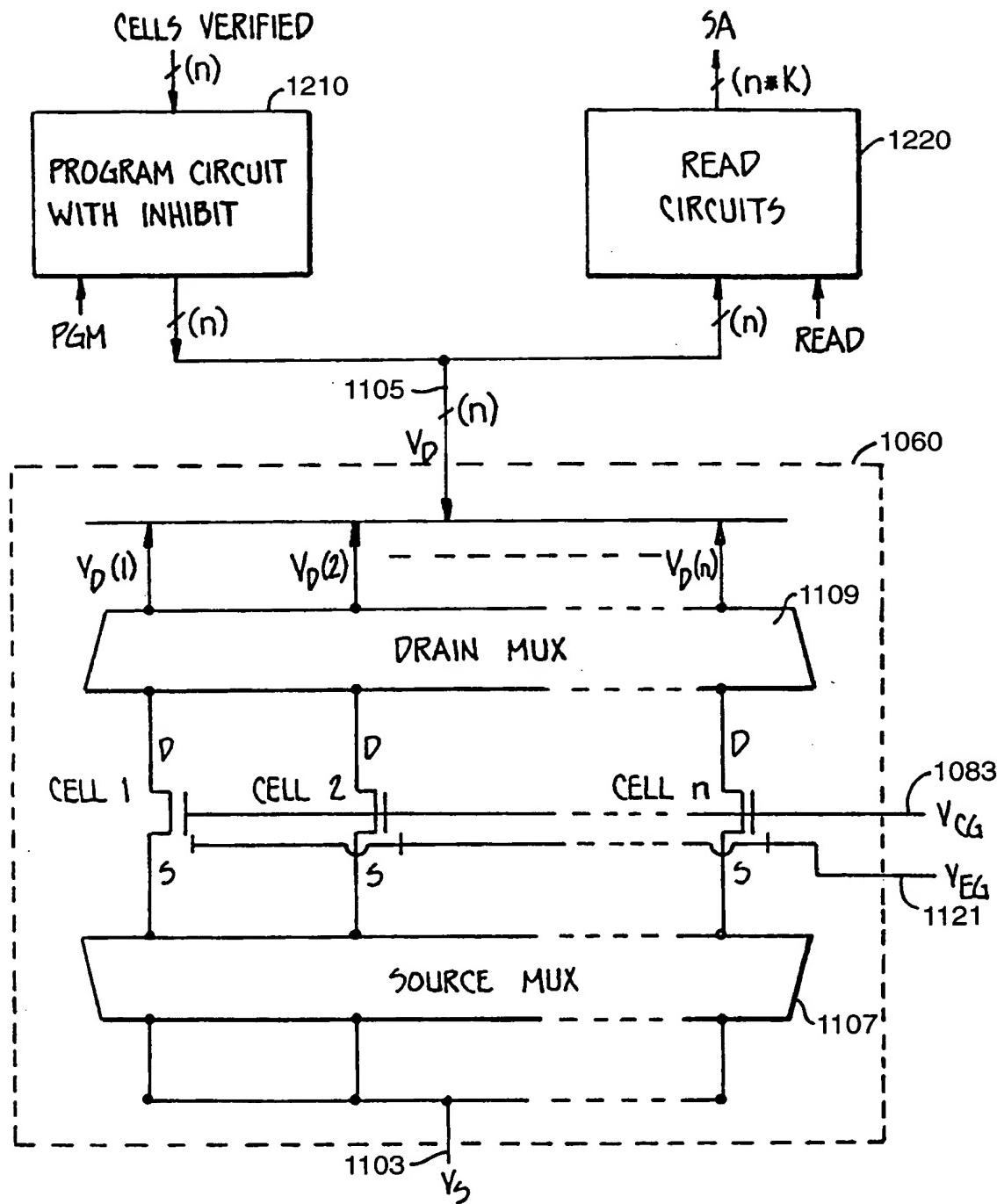
FIG._21A

00000000000000000000000000000000

- (1) LOCAL REF. CELLS ARE PREVIOUSLY PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CELLS
- (2) RELATIVE TO THE LOCAL REFERENCE CELLS READ THE MASTER REF. CELLS
- (3) DETERMINE THE DIFFERENCES, IF ANY AND BIAS. THE MASTER REF CELLS' CURRENTS SUCH THAT THE SAME READING IS OBTAINED RELATIVE TO THE BIASED MASTER REF. CELLS AS RELATIVE TO THE LOCAL REF. CELLS
- (4) RELATIVE TO THE BIASED MASTER REF. CELLS, READ THE ADDRESSED CELLS

FIG._21D

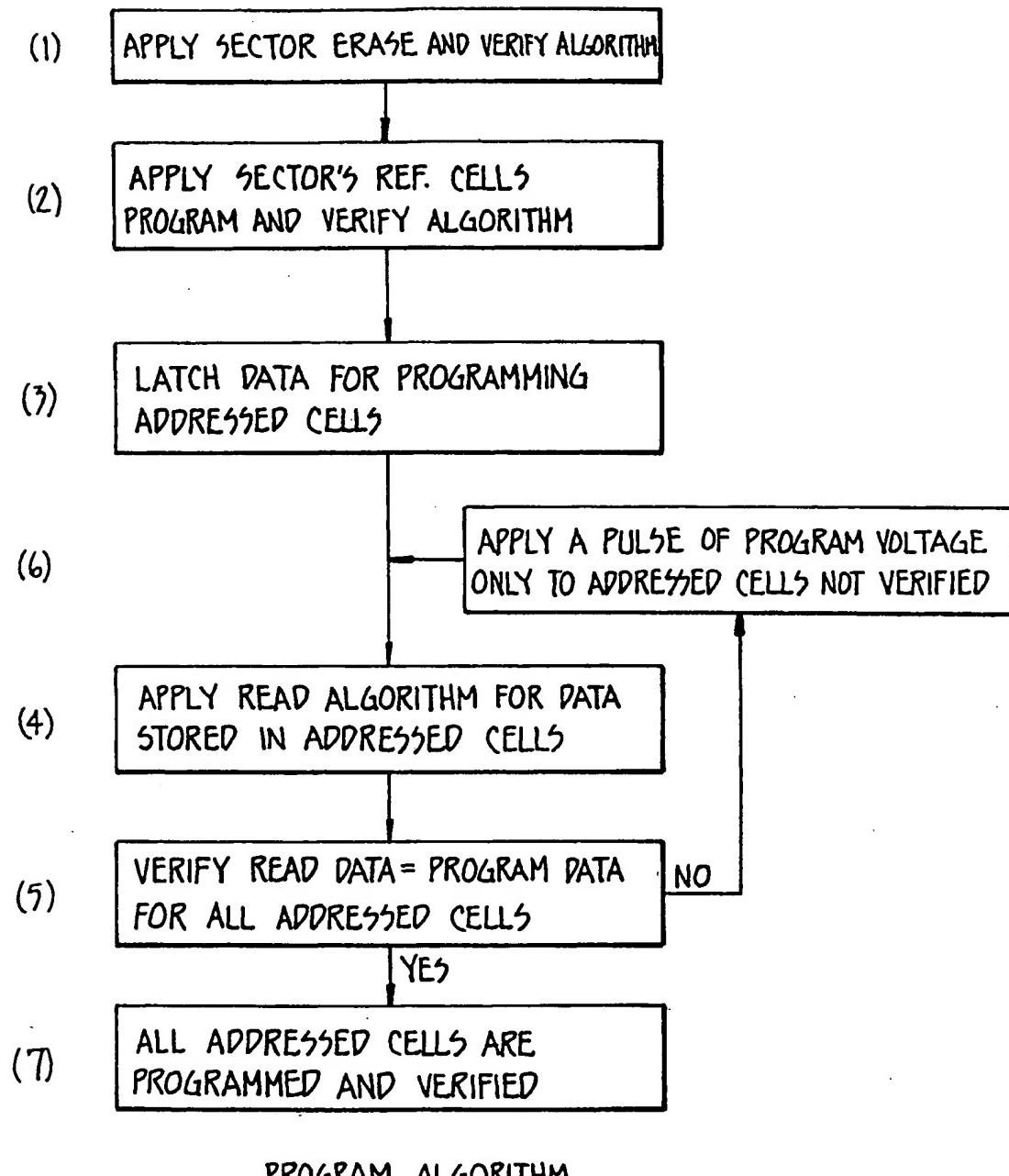
**FIG._21B****FIG._21C**

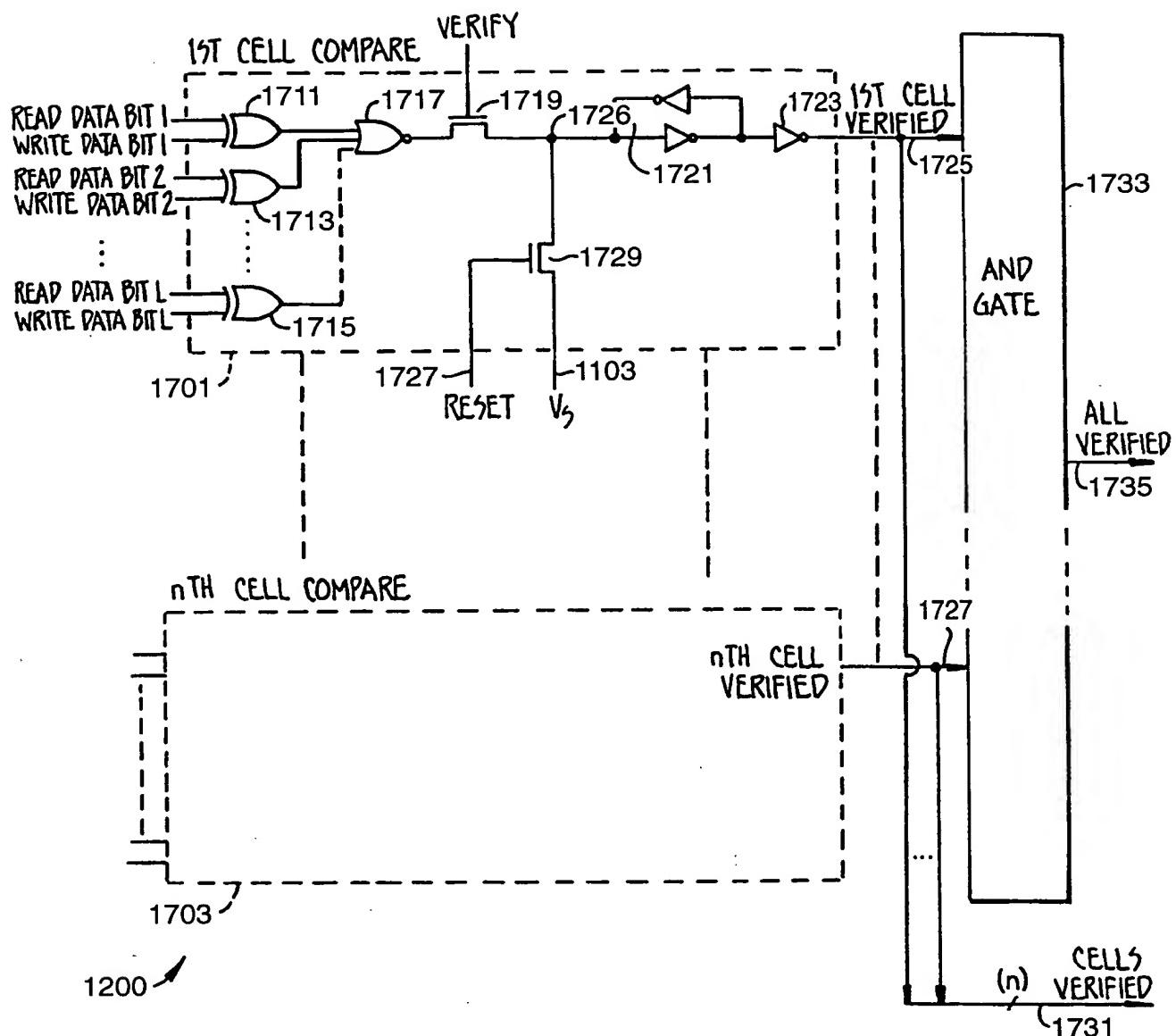


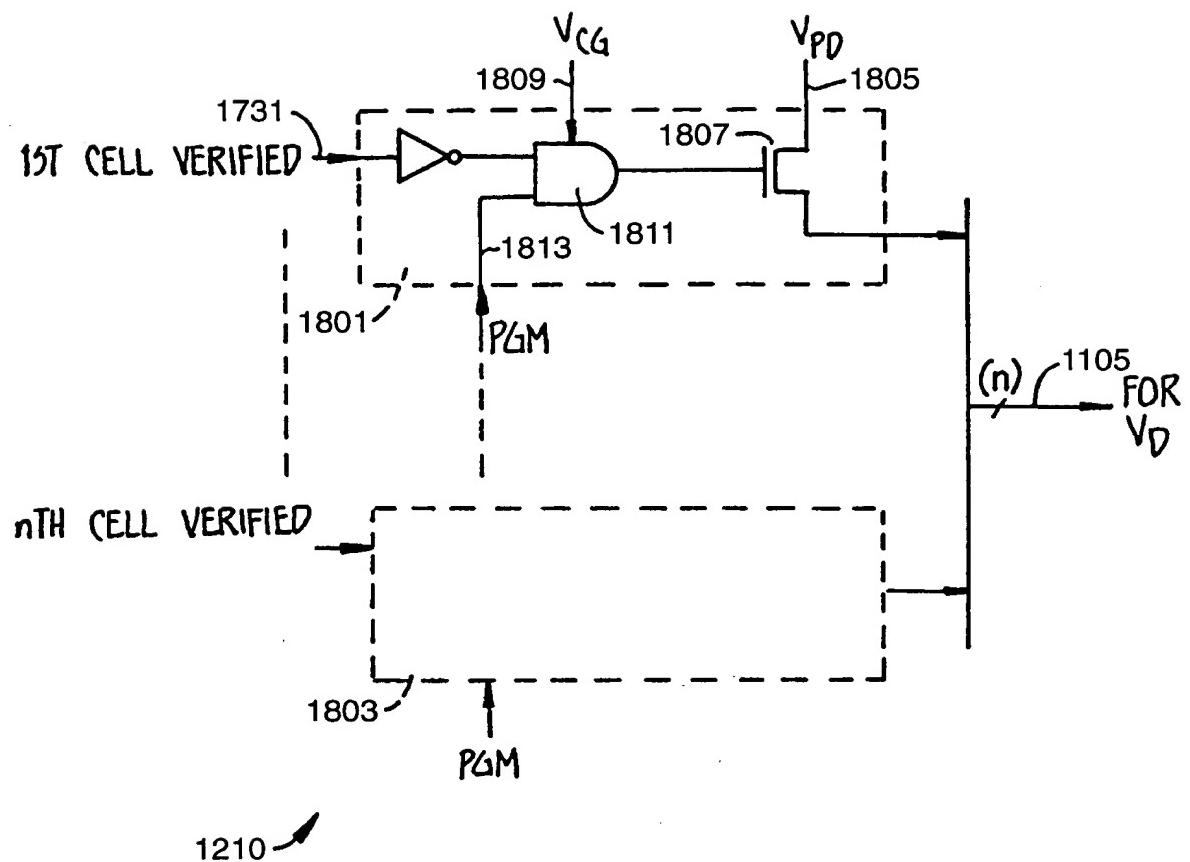
READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG._22

TOP SECRET - DEFENSE

**FIG._23**

**FIG._24**

**FIG._25**

	SELECTED CONTROL GATE V_{CG}	DRAIN V_D	SOURCE V_S	ERASE GATE V_{EG}
READ	V_{PG}	V_{REF}	V_{SS}	V_E
PROGRAM	V_{PG}	V_{PD}	V_{SS}	V_E
PROGRAM VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E

TABLE 1**FIG._26**

(TYPICAL) VALUES	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V_{PG}	V_{CC}	12V	$V_{CC} + \delta V$	V_{CC}	$V_{CC} - \delta V$
V_{CC}	5V	5V	5V	5V	5V
V_{PD}	V_{SS}	8V	8V	V_{SS}	V_{SS}
V_E	V_{SS}	V_{SS}	V_{SS}	20V	V_{SS}
UNSELECTED CONTROL GATE	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
UNSELECTED BIT LINE	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}

$$V_{SS} = 0V, \quad V_{REF} = 1.5V, \quad \delta V = 0.5V - 1V$$

TABLE 2**FIG._27**